

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method for improved differential electrical noise reduction for an integrated circuit device having a memory having multiple vertical levels of circuitry, the memory having at least four arrays of memory cells, each array of memory cells being substantially equally spaced from an adjacent array of memory cells, each array of memory cells including a plurality of memory cells and at least four pairs of digitlines, each pair of digitlines including a first digitline and a second digitline, the first digitline and the second digitline being substantially vertically aligned in an upper conductive level and a lower conductive level of the integrated circuit device, the first digitline and second digitline of each pair of digitlines each connected to an equal number of the memory cells in each array of memory cells, the method comprising:

electrically balancing the first digitline and the second digitline of each digitline pair of the at least four pairs of digitlines to balance the electrical noise therebetween by vertically twisting the first digitline and the second digitline of each pair of digitlines of the at least four pairs of digitlines between arrays of the at least four arrays of memory cells in a twist region located between each array of the at least four arrays of memory cells, a first pair of digitlines and a third pair of digitlines of the at least four pairs of digitlines vertically twisted in the twist region located between a first array of memory cells and a second array of memory cells and vertically twisted in the twist region located between a third array of memory cells and a fourth array of memory cells while a second pair of digitlines and a fourth pair of digitlines of the at least four pairs of digitlines are vertically twisted in the twist region located between the second array of memory cells and the third array of memory cells, the electrically balancing including connecting an equal number of memory cells to a portion of one of the first digitline and the second digitline of a pair of digitlines of the at least four pairs of digitlines when located in a lower conductive level of an array of the at least four arrays of memory cells.

2. (Previously Presented) The method of claim 1, further comprising:
isolating adjacent memory cells of an array of the at least four arrays of memory cells using an
isolation region comprising a plurality of isolation transistors, each isolation transistor
having a gate biased to a predetermined voltage.